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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant: Kayvan Sadra, et al. Docket Number: TI-35961

Serial No.: 10/694,237 Art Unit: 2813

Filed: 10/27/03 Examiner: Laura M. Schillinger

For: Application of Different Isolation Schemes for Logic and Embedded Memory

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___ CONTINUATION APP'N	
___ DIVISIONAL APP'N	

NAME OF INVENTOR(S): Kayvan Sadra, et al.	RECEIPT DATE & SERIAL NO.: **Serial No.: 10/694,237** **Filing Date:** 10/27/03
TITLE OF INVENTION: Application of Different Isolation Schemes for Logic and Embedded Memory	
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Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, TX 75265-5474

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kayvan Sadra, et al. **Art Unit: 2813**

Serial No.: 10/694,237 **Examiner: Laura M. Schillinger**

Filed: 10/27/03 **Docket: TI-35961**

For: APPLICATION OF DIFFERENT ISOLATION SCHEMES FOR LOGIC AND EMBEDDED MEMORY

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Karen Vertz 12-6-05
Karen Vertz Date

Transmitted herewith is an Appeal Brief in the above-identified application. The Commissioner is hereby authorized to charge the ***$500.00*** fee for this appeal, or credit any overpayment to Account No. 20-0668.

Respectfully submitted,

Rose Alyssa Keagy
Registration No. 35,095

Texas Instruments, Incorporated
P. O. Box 655474 - M/S 3999
Patent Department
Dallas, Texas 75265

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Sadra et al.

Docket No.: TI-35961

Serial No.: 10/694,237

Art Unit: 2813

Filed: 10/27/2003

Examiner: Schillinger, L.

Confirmation No.:2682

Title: Application of Different Isolation Schemes For Logic And Embedded Memory

APPEAL BRIEF UNDER 37 CFR §1.192

December 6, 2005

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
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Karen Vertz — Karen Vertz

12-6-05 — Date

Dear Sir:

Pursuant to the final Office Action mailed 07/27/2005, the Appellants submit this Appellants' Brief. The Commissioner is hereby requested and authorized to charge any fees necessary for the filing of the enclosed papers to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

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TABLE OF CONTENTS

REAL PARTY IN INTEREST

The Real Party in Interest in the present appeal is Texas Instruments Incorporated, the assignee, as evidenced by the assignment set forth at Reel 014643, Frame 0792.

RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to the Appellants.

STATUS OF CLAIMS

Claims 1-12 are the subject of this appeal. Claims 1-28 are pending, Claims 1-12 are rejected, Claims 13-25 are withdrawn under a traversed restriction requirement, and Claims 26-28 are withdrawn as being drawn to a non-elected invention.

STATUS OF AMENDMENTS

The Appellants did not file any amendment subsequent to the final Office Action dated July 27, 2004.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent Claim 1 is directed to a method of fabricating a semiconductor device (element 300 of FIG. 3, page 11 lines 3-4, element 900 of FIG. 9, element 1500 of FIG. 15). The method includes forming first type well regions (element 302 of FIG. 3, page 11 line 20 through page 12 line 7, FIG. 5, element 902 of FIG. 9, element 1502 of FIG. 15) within a core logic portion (element 406 of FIG. 5, element 1006 of FIG. 13, element 1606 of FIG. 19) and an embedded transistor-containing memory portion (element 404 of FIG. 5, element 1004 of FIG. 13, element 1604 of FIG. 19) of the device. The method also includes forming second type well regions (element 304 of FIG. 3, page 12 lines 8-19, FIG. 6, element 904 of FIG. 9, element 1504 of FIG. 15) within the core logic portion (element 406 of FIG. 6, element 1006 of FIG. 13, element 1606 of FIG. 19) and the embedded transistor-containing memory portion (element 404 of FIG. 6, element 1004 of FIG. 13, element 1604 of FIG. 19) of the device. Moreover, the method includes performing a supplemental isolation implant (element 306 of FIG. 3, page 12 line 20 through page 13 line 4, FIG. 7, element 906 of FIG. 9, element 1508 of FIG. 15) within at least one of the first type well regions of the embedded transistor-containing memory portion (element 404 of FIG. 7, element 1004 of FIG. 13, element 1604 of FIG. 19) to modify dopant profile(s) (page 13 line 24 through page 14 line 2) of the at least one of the first type well regions (element 726 of FIG. 7, page 13 lines 1-3, element 1112 of FIG. 11, element 1712 of FIG. 17) to increase isolation (page 13 line 24 through page 14 line 2).

Claim 2 is dependent on Claim 1 and specifies an additional step of performing a supplemental isolation implant (element 308 of FIG. 3, page 13 lines 5-18, FIG. 8) within at least one of the second type well regions to modify dopant profile(s) (page 13 line 24 through page 14 line 2) of the at least one of the second type well regions (element 830 of FIG. 8, page 13 lines 8-10) to increase isolation (page 13 line 24 through page 14 line 2).

Claim 3 is dependent on Claim 2 and further specifies that the (page 6 line 22) first type well regions are n-type (page 13 lines 18-19, element 304 of FIG. 3, element 622 of FIG. 6, page 12 lines 13-14) and the second type well regions are p-type (page 13 lines 18-19, element 302 of FIG. 3, element 508 of FIG. 5, page 12 line 2).

Claim 4 is dependent on Claim 2 and further specifies that the first type well regions are p-type (page 13 lines 18-19, element 302 of FIG. 3, element 508 of FIG. 5, page 12 line 2) and the second type regions are n-type (page 13 lines 18-19, element 304 of FIG. 3, element 622 of FIG. 6, page 12 lines 13-14).

Claim 5 is dependent on Claim 1 and specifies the additional steps of forming first shallow trench isolation regions (element 510 of FIGS. 5-8, page 11 lines 26-29) having a first width (element 832 of FIG. 8, page 13 line 26) that separate active regions across well boundaries (elements 508 and 622 of FIG. 8) within the core logic portion

(element 406 of FIGS. 5-8) and forming second shallow trench isolation regions (element 512 of FIGS. 5-8, page 11 lines 26-29) having a second width (element 831 of FIG. 8, page 13 lines 24-25) that separate active regions across well boundaries (elements 726 and 830 of FIG. 8) within the embedded transistor-containing memory portion (element 404 of FIGS. 5-8).

Claim 6 is dependent on Claim 5 and further specifies that the second width is less than the first width (page 2 lines 18-28, page 10 lines 14-15, FIG. 2, page 13 lines 24-27, FIG. 8).

Claim 7 is dependent on Claim 5 and further specifies that the second width is substantially less than the first width (page 2 lines 18-28, page 13 lines 24-27, FIG. 8).

Claim 8 is dependent on Claim 1 and specifies the step of forming stacked gate structures prior to performing a supplemental isolation implant (page 11 lines 12-13, page 13 line 21, element 1506 of FIG. 15, element 1936 of FIG. 19, page 19 lines 21-23).

Claim 9 is dependent on Claim 1 and further specifies that performing a supplemental isolation implant within the first type well regions of the embedded transistor-containing memory portion (element 306 of FIG. 3, page 12 line 20 through page 13 line 4, element 906 of FIG. 9, element 1508 of FIG. 15) comprises forming a

layer of resist (element 403 of FIGS. 7 and 4, page 12 lines 26-27, element 1120 of FIG. 11, element 1720 of FIG. 17) on the device and selectively exposing (page 12 line 24 through page 13 line 4, FIGS. 7, 11, 17, and 27-32) the first type well regions (element 726 of FIG. 7, page 12 lines 25-26, element 1112 of FIG. 11, element 1712 of FIG. 17) of the embedded transistor-containing memory (element 404 of FIG. 7, element 1004 of Fl. 11, element 1604 of FIG. 17); and implanting one or more dopants of the first type (element 724 of FIG. 7, page 12 line 24, element 1122 of FIG. 11, element 1722 of FIG. 17) into the exposed first type well regions (element 726 of FIG. 7, page 12 lines 24-27, element 1112 of FIG. 11, element 1712 of FIG. 17).

Claim 10 is dependent on Claim 9 and further specifies that the layer of resist formed is also employed to raise a threshold voltage of high-threshold-voltage transistors formed on the device (FIG. 9, page 14 lines 3-19, FIG. 15, page 17 lines 21-24, page 18 lines 4-9).

Claim 11 is dependent on Claim 10 and further specifies that the threshold voltage of the high-threshold-voltage transistors is raised using a channel implant (FIG. 13, page 14 lines 3-7 and 16-19, page 16 lines 6-17).

Claim 12 is dependent on Claim 10 and further specifies that the threshold voltage of the high-threshold-voltage transistors is raised using a pocket implant (FIG. 19, page 18, page 19 line 27 through page 20 line 5).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-12 stand rejected under 35 U.S.C. §102(b) as anticipated by the patent granted to Dennison (U.S. Pat. No. 6,593,176).

ARGUMENT

Rejection under 35 U.S.C. §102(b) over the patent granted to Dennison (U.S. Pat. No. 6,593,176).

Claim 1

Independent Claim 1 positively recites performing a supplemental isolation implant within at least one of the first type well regions of the embedded transistor-containing memory portion to modify dopant profile(s) of the at least one of the first type well regions to increase isolation. These advantageously claimed features are not taught or suggested by the patent granted to Dennison.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements that by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the

advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

Therefore, Claim 1 is patentable over the patent granted to Dennison.

Claim 2

Claim 2 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 2 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Dennison. Namely, Claim 2 further specifies the additional step of performing a supplemental isolation implant within at least one of the second type well regions to modify dopant profile(s) of the at least one of the second type well regions to increase isolation.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and

column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

The Appellants respectfully traverse the statement in the Office Action (page 3) that Dennison teaches the features of the Appellants' Claim 2 in column 5 lines 5-15. Specifically, the Office Action states (at the top of page 3) that column 5 lines 5-15 teach a supplemental implant of the first type well region. Immediately following that assertion, the Office Action states that the same section of Dennison (column 5 lines 5-15) teaches a supplemental implant of the second type well implant. The Appellants submit that column 5 lines 5-15 cannot teach a supplemental isolation implant of both the first type and the second type well regions.

Therefore, Claim 2 is patentable over the patent granted to Dennison.

Claim 3

Claim 3 is dependent on Claim 2 and is therefore allowable for the same reasons that Claims 1 and 2 are allowable. Furthermore, Claim 3 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claims 1 and 2, are not taught nor suggested by the patent granted to

Dennison. Namely, Claim 3 further specifies the additional limitation that the first type well regions are n-type and the second type well regions are p-type.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

In addition, the Appellants submit that Dennison teaches away from the advantageously claimed invention where the first type well regions can be either n-type or p-type (and the same with the second type well region). The Appellants submit that the n-type well region is stated to be discussed in column 5 lines 30-40 in paragraphs 3 and 4 of page 3 of the Office Action. Therefore - as the Office Action states - Dennison does not teach that a specified well region is either n-type or p-type as advantageously claimed in the Appellants Claims 3 and 4.

Therefore, Claim 3 is patentable over the patent granted to Dennison.

Claim 4

Claim 4 is dependent on Claim 2 and is therefore allowable for the same reasons that Claims 1 and 2 are allowable. Furthermore, Claim 4 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claims 1 and 2, are not taught nor suggested by the patent granted to Dennison. Namely, Claim 4 further specifies the additional limitation that the first type well regions are p-type and the second type well regions are n-type.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

In addition, the Appellants submit that Dennison teaches away from the advantageously claimed invention where the first type well regions can be either n-type or p-type (and the same with the second type well region). The Appellants submit that the n-type well region is stated to be discussed in column 5 lines 30-40 in paragraphs 3 and 4 of page 3 of the Office Action. Therefore - as the Office Action states - Dennison does not teach that a specified well region is either n-type or p-type as advantageously claimed in the Appellants Claims 3 and 4.

Therefore, Claim 4 is patentable over the patent granted to Dennison.

Claim 5

Claim 5 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 5 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Dennison. Namely, Claim 5 further specifies the additional steps of forming first shallow trench isolation regions having a first width that separate active regions across well boundaries within the core logic portion and forming second shallow trench isolation regions having a second width that separate active regions across well boundaries within the embedded transistor-containing memory portion.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

In addition, the Appellants respectfully traverse the assertion in the Office Action (page 3) that Dennison teaches the use of different shallow trench isolation widths in columns 6-7 lines 55-45. The Appellants respectfully submit that in column 6 line 55 through column 7 line 45 that just the memory array 102 is discussed (FIGS. 9-10a, column 2 lines 37-49, column 5 lines 64-66, column 6 line 21-22, note that element 102 of FIGS. 9-10a is the memory array – see column 4 line 53). Therefore, Dennison does not teach the use of different shallow trench isolation widths between the core logic and the memory portion as advantageously claimed (column 4 lines 34-52, FIGS. 2-6).

Therefore, Claim 5 is patentable over the patent granted to Dennison.

Claim 6

Claim 6 is dependent on Claim 5 and is therefore allowable for the same reasons that Claim 5 is allowable. Furthermore, Claim 6 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claims 1 and 5, are not taught nor suggested by the patent granted to Dennison. Namely, Claim 6 further specifies the additional limitation that the second width is less than the first width.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

In addition, the Appellants respectfully traverse the assertion in the Office Action (page 3) that Dennison teaches the use of different shallow trench isolation widths in

columns 6-7 lines 55-45. Furthermore, the Appellants respectfully traverse the assertion in the Office Action (page 4) that Dennison teaches that the second width is less than the first shallow trench isolation width in columns 6-7 lines 55-45. The Appellants respectfully submit that in column 6 line 55 through column 7 line 45 that just the memory array 102 is discussed (FIGS. 9-10a, column 2 lines 37-49, column 5 lines 64-66, column 6 line 21-22, note that element 102 of FIGS. 9-10a is the memory array – see column 4 line 53). Therefore, Dennison does not teach the use of different shallow trench isolation widths between the core logic and the memory portion as advantageously claimed (column 4 lines 34-52, FIGS. 2-6). Moreover, Dennison does not teach that the width of the shallow trench isolation structures in the memory portion is less than the width of the shallow trench isolation structures in the core logic portion, as advantageously claimed in Claim 6 (column 4 lines 34-52, FIGS. 2-6).

Therefore, Claim 6 is patentable over the patent granted to Dennison.

Claim 7

Claim 7 is dependent on Claim 5 and is therefore allowable for the same reasons that Claim 5 is allowable. Furthermore, Claim 7 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claims 1 and 5, are not taught nor suggested by the patent granted to Dennison.

Namely, Claim 7 further specifies the additional limitation that the second width is substantially less than the first width.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

In addition, the Appellants respectfully traverse the assertion in the Office Action (page 3) that Dennison teaches the use of different shallow trench isolation widths in columns 6-7 lines 55-45. Furthermore, the Appellants respectfully traverse the assertion in the Office Action (page 4) that Dennison teaches that the second width is substantially less than the first shallow trench isolation width in columns 6-7 lines 55-45. The Appellants respectfully submit that in column 6 line 55 through column 7 line 45 that just the memory array 102 is discussed (FIGS. 9-10a, column 2 lines 37-49, column 5 lines 64-66, column 6 line 21-22, note that element 102 of FIGS. 9-10a is the memory array

– see column 4 line 53). Therefore, Dennison does not teach the use of different shallow trench isolation widths between the core logic and the memory portion as advantageously claimed (column 4 lines 34-52, FIGS. 2-6). Moreover, Dennison does not teach that the width of the shallow trench isolation structures in the memory portion is substantially less than the width of the shallow trench isolation structures in the core logic portion, as advantageously claimed in Claim 7 (column 4 lines 34-52, FIGS. 2-6).

Therefore, Claim 7 is patentable over the patent granted to Dennison.

Claim 8

Claim 8 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 8 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Dennison. Namely, Claim 8 further specifies the additional step of forming stacked gate structures prior to performing a supplemental isolation implant.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24, column 4 line 53

through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

In addition, the Appellants respectfully traverse the statement in the Office Action (page 4) that Dennison teaches forming the stacked gate structures prior to performing the supplemental isolation implant. The Appellants submit that on page 3 the Office Action states that the supplemental isolation implant is discussed in column 5 lines 5-15. The Appellants submit that the gate stacks are discussed later in the Dennison patent (e.g. after the isolation implant step). Furthermore, Dennison does not state (and the Office Action does not show) forming stacked gate structures prior to performing the supplemental isolation implant as advantageously claimed.

Therefore, Claim 8 is patentable over the patent granted to Dennison.

Claim 9

Claim 9 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 9 is allowable on its own merits because it

recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Dennison. Namely, Claim 9 further specifies the additional limitation that the supplemental isolation implant within the first type well regions of the embedded transistor-containing memory portion comprises forming a layer of resist on the device and selectively exposing the first type well regions of the embedded transistor-containing memory; and implanting one or more dopants of the first type into the exposed first type well regions.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

In addition, the Appellants are confused by the statement in the Office Action (page 4) that Dennison teaches the limitations of Claim 9 in FIG. 3. The Appellants submit that previously (on page 3) the Office Action stated that the supplemental isolation

implant is discussed in column 5 lines 5-15 (which relates to fabrication of the memory array in FIG. 2). Therefore, Dennison cannot also teach the supplemental isolation implant step in FIG. 3 (in addition to column 5 lines 5-15 and FIG. 2), as stated on page 4 of the Office Action. Moreover, the Appellants submit that Dennison shows the fabrication of the peripheral logic in FIG. 3 (column 5 lines 25-30), not an implant within the memory portion as advantageously claimed.

Therefore, Claim 9 is patentable over the patent granted to Dennison.

Claim 10

Claim 10 is dependent on Claim 9 and is therefore allowable for the same reasons that Claims 1 and 9 are allowable. Furthermore, Claim 10 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claims 1 and 9, are not taught nor suggested by the patent granted to Dennison. Namely, Claim 10 further specifies the additional limitation that the layer of resist formed is also employed to raise a threshold voltage of high-threshold-voltage transistors formed on the device.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements -

which by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

The Appellants are confused by the statement in the Office Action (page 4) that Dennison teaches the limitations of Claim 10 in FIG. 3. The Appellants submit that FIG. 3 does not teach or suggest the use of high-threshold-voltage transistors (column 5 lines 25-30).

Therefore, Claim 10 is patentable over the patent granted to Dennison.

Claim 11

Claim 11 is dependent on Claim 10 and is therefore allowable for the same reasons that Claims 1, 9, and 10 are allowable. Furthermore, Claim 11 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claims 1, 9, and 10, are not taught nor suggested by the patent granted to Dennison. Namely, Claim 11 further specifies the additional limitation that the

threshold voltage of the high-threshold-voltage transistors is raised using a channel implant.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

The Appellants are confused by the statement in the Office Action (page 4) that Dennison teaches the limitations of Claim 11 in FIG. 3. The Appellants submit that FIG. 3 does not teach or suggest the use of high-threshold-voltage transistors or the step of a channel implant (column 5 lines 25-30).

Therefore, Claim 11 is patentable over the patent granted to Dennison.

Claim 12

Claim 12 is dependent on Claim 10 and is therefore allowable for the same reasons that Claims 1, 9, and 10 are allowable. Furthermore, Claim 12 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claims 1, 9, and 10, are not taught nor suggested by the patent granted to Dennison. Namely, Claim 12 further specifies the additional limitation that the threshold voltage of the high-threshold-voltage transistors is raised using a pocket implant.

Dennison does not teach the advantageously claimed invention because Dennison does not teach a method of fabricating a transistor-containing memory. Rather, Dennison only teaches the fabrication of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24, column 4 line 53 through column 5 line 15). As shown in Dennison FIG. 1, the Dennison memory element consists of a phase-change element (denoted by the circle) and an isolating diode (denoted by the triangle), but no transistor. See also FIG. 20 of Dennison and column 13 line 55 though column 14 line 31. Moreover, Dennison teaches away from the advantageously claimed invention by teaching that the transistors are only located in the 'peripheral logic' (element 104) of substrate 100 (column 5 line 18, FIGS. 2-4).

The Appellants are confused by the statement in the Office Action (page 5) that Dennison teaches the limitations of Claim 12 in FIG. 3. The Appellants submit that FIG. 3

does not teach or suggest the use of high-threshold-voltage transistors or the step of a pocket implant (column 5 lines 25-30).

Therefore, Claim 12 is patentable over the patent granted to Dennison.

ADDITIONAL AGRUMENTS

In response to the statements in the 'Response to Arguments' section of the Office Action, the Appellants respectfully traverse the assertion that Dennison teaches transistor containing memory elements in FIGS. 2 and 4. Specifically, the Office Action points to the presence of PMOS and NMOS structures in FIGS. 2 and 4. The Appellants submit that the PMOS structure is formed in FIG. 3 in the peripheral logic portion (element 102) of the substrate and the NMOS structure is formed in FIG. 4 in the peripheral logic portion (element 102) of the substrate (column 5 lines 25-42). Dennison does not teach the use of PMOS and NMOS structures in the memory array (element 102), as stated in the Office Action.

CONCLUSION

For the reasons stated above, the Appellants respectfully contend that each claim is patentable. Therefore, the reversal of all rejections is courteously solicited.

Respectfully submitted,

Rose Alyssa Keagy

Attorney for Appellants

Reg. No. 35,095

Texas Instruments Incorporated

PO BOX 655474, M/S 3999

Dallas, TX 75265

972/917-4167

FAX - 972/917-4409/4418

CLAIMS APPENDIX

1. A method of fabricating a semiconductor device comprising:

forming first type well regions within a core logic portion and an embedded transistor-containing memory portion of the device;

forming second type well regions within the core logic portion and the embedded transistor-containing memory portion of the device;

performing a supplemental isolation implant within at least one of the first type well regions of the embedded transistor-containing memory portion to modify dopant profile(s) of the at least one of the first type well regions to increase isolation.

2. The method of claim 1, further comprising performing a supplemental isolation implant within at least one of the second type well regions to modify dopant profile(s) of the at least one of the second type well regions to increase isolation.

3. The method of claim 2, wherein the first type well regions are n-type and the second type well regions are p-type.

4. The method of claim 2, wherein the first type well regions are p-type and the second type regions are n-type.

5. The method of claim 1, further comprising forming first shallow trench isolation regions having a first width that separate active regions across well boundaries within the core logic portion and forming second shallow trench isolation regions having a second width that separate active regions across well boundaries within the embedded transistor-containing memory portion.

6. The method of claim 5, wherein the second width is less than the first width.

7. The method of claim 5, wherein the second width is substantially less than the first width.

8. The method of claim 1, further comprising forming stacked gate structures prior to performing a supplemental isolation implant.

9. The method of claim 1, wherein performing a supplemental isolation implant within the first type well regions of the embedded transistor-containing memory portion comprises:

forming a layer of resist on the device and selectively exposing the first type well regions of the embedded transistor-containing memory; and

implanting one or more dopants of the first type into the exposed first type well regions.

10. The method of claim 9, wherein the layer of resist formed is also employed to raise a threshold voltage of high-threshold-voltage transistors formed on the device.

11. The method of claim 10, wherein the threshold voltage of the high-threshold-voltage transistors is raised using a channel implant.

12. The method of claim 10, wherein the threshold voltage of the high-threshold-voltage transistors is raised using a pocket implant.